THERMO-FLUID-STRESS ANALYSIS OF TWO-LAYER MICROCHANNELS FOR COOLING CHIPS WITH HOT SPOTS

Abas Abdoli, George S. Dulikravich, Genesis Vasquez and Siavash Rastkar
Department of Mechanical and Materials Engineering, MAIDROC Laboratory, Florida International University, Miami, FL 33174, aabdo004@fiu.edu, dulikrav@fiu.edu, gvasq007@fiu.edu, srast002@fiu.edu

ABSTRACT

Two-layer single phase flow microchannels were studied for cooling of electronic chips with a hotspot. A chip with 2.45 x 2.45 mm footprint and a hot spot of 0.5 x 0.5 mm in its center was studied in this research. Two different cases were simulated in which heat fluxes of 1500 W cm\(^{-2}\) and 2000 W cm\(^{-2}\) were applied at the hot spot. Heat flux of 1000 W cm\(^{-2}\) was applied on the rest of the chip. Each microchannel layer had 20 channels with aspect ratio of 4 to 1. Direction of the second microchannel layer was rotated 90 degrees with respect to the first layer. Fully 3-D conjugate heat transfer analysis was performed to study the heat removal capacity of the proposed two-layer microchannel cooling design for high heat flux chips. In the next step, a linear stress analysis was performed to investigate the effects of thermal stresses applied to the microchannel cooling design due to variations of temperature field.

Key Words: Electronics Cooling, Single Phase Flow Microchannel, Hot Spot.

1. INTRODUCTION

Thermal management challenges facing electronic cooling developers [1,2] are currently at the confluence of chip power dissipation well above 100 W cm\(^{-2}\) as background heat flux, and localized hot spots with more than 1000 W cm\(^{-2}\) fluxes.

Shau et al. [3] applied a hybrid cooling scheme which combines microfluidic and solid-state cooling techniques in cooling hotspots with heat flux close to 250 W cm\(^{-2}\). In another research, Shau et al. [4] studied a liquid-thermoelectric hybrid cooling method for hot spots with heat fluxes more than 600 W cm\(^{-2}\). They reported that liquid-thermoelectric hybrid cooling showed better results for higher heat fluxes at hot spots. Alfier et al. [5] numerically investigated hot spot cooling in 3-D stacked chips with integrated cooling. They studied the influence and implications of the integrated water-cooling, Through-Silicon-Via (TSV) distribution, and size on the control of inhomogeneous hot spots. Zhang et al. [6,7] experimentally investigated effects of silicon micro pin-fin heat sink with integrated TSVs in cooling high power chips.

One of the first vestiges of the application of optimization methods to improve cooling channel geometries was in the inverse design and optimization of internally cooled gas turbine blades. Martin and Dulikravich [8] presented this type of a fully automated program and validated it against experimental results from Pratt & Whitney Aircraft Company. They also used this solver for microchannel electronics cooling [9,10]. A few years later, Jelisavcic et al. [11] applied hybrid evolutionary optimization to the same concept of channel network optimization for turbo-machinery applications. Subsequently, Gonzales et al. [12] executed relevant work comprising 2D microchannel networks optimization. Genetic algorithms have been used by Wei and Joshi [13] to perform single objective optimization in order to minimize overall thermal resistance. Husain and Kim [14] performed single objective optimization using response surface approximation in order to find optimal microchannel width, depth and fin width.

Abdoli and Dulikravich [5] performed multi objective optimization for 4-layer branching microchannel configurations with 67 design variables to improve heat removal and decrease
temperature non-uniformity and coolant pumping pressure drop. They also numerically optimized the multi-layer through-flow microchannels for uniform heat flux of 800 W cm$^{-2}$ [16].

In the present paper, a cooling configuration with two layers of straight microchannels was investigated numerically. The main advantages of using straight through-flow cooling channels rather than branching cooling channels are: a) lower pumping power requirements, b) lower manufacturing cost, c) better uniformity of hot surface temperature; and d) higher reliability in case of blockage in any of the microchannels.

2. TWO-LAYER COOLING DESIGN INCLUDING A HOT SPOT

A two-layer microchannel configuration was designed for a chip with 2.45 x 2.45 mm footprint, shown in figure 1. Each microchannel layer consists of 20 channels. Each channel has the cross section dimension of 60 x 60 µm. As this figure shows, direction of the second layer was rotated 90 degrees with respect to the first layer. Substrate, first and second layers of microchannels were all assumed to be made from silicon. A hot spot with size of 500 x 500 µm was located at the center of the substrate top surface.

![Figure 1. Expanded view of two-layer microchannel cooling design.](image)

COMSOL Multiphysics software was used for meshing the configuration. This cooling design configuration consists of forty fluid domains and one solid domain. A fine 3D hybrid computational grid was used for finite element simulations. Each of the 40 microchannels was discretized with 20,000 3D grid cells and the rest of the cooling design was discretized with 600,000 3D grid cells.

Figure 2 illustrates the hybrid grid in the entire solution domains. The enlarged view demonstrates the concentration of grid cells near edges. In this study, considering the applied Reynolds number (< 290), flow pattern inside microchannels was assumed to be laminar [17]. Therefore, not having a very fine mesh adjacent to the internal walls was acceptable since the flow was not turbulent.

![Figure 2. Hybrid computational grid with an enlarged view](image)
3. CONJUGATE HEAT TRANSFER ANALYSIS

Multi-domain steady state conjugate heat transfer analysis was performed to study the temperature distribution using a two-layer microchannel configuration. As mentioned above, forty fluid domains and one solid domain were coupled and simulated using COMSOL Multiphysics conjugated heat transfer finite element solver. Water was used as the cooling liquid. Inlet averaged velocity was assumed to be 2 m s\(^{-1}\). Hydraulic diameter was calculated as the square root of cross section area \([18]\). Therefore, the inlet Reynolds number was 287.4. The water inlet temperature was set to +26.8 °C. The outlet static pressure was specified as 110 kPa. Two different cases were simulated. In case 1, a uniform thermal load of 1500 W cm\(^{-2}\) was applied at the hot spot. In case 2, a uniform heat flux of 2000 W cm\(^{-2}\) was applied to the hot spot. Thermal boundary conditions were:

1. Constant bottom surface temperature: +26.8 °C
2. Constant background heat flux (excluding hot spot): 1000 W cm\(^{-2}\)
3. Constant heat flux on hot spot, case 1: 1500 W cm\(^{-2}\) and case 2: 2000 W cm\(^{-2}\)
4. Adiabatic surface for all sidewalls.

Figure 3a illustrates the calculated temperature distribution inside the substrate and coolant for case 1. The water flow direction in the first layer was in the x-direction. In the second layer, due to a 90 degree rotation with respect to the first layer, water was pumped in the direction of z-axis. As figure 3a illustrates, temperature variations in the second microchannel layer were not significant. In other words, this layer did not play a noticeable role in this cooling system. As water moves toward the outlets, its temperature increases. Figure 3b shows variations of temperature on the top surface of silicon substrate. Due to the 90 degree shift in the flow directions, a lower temperature zone can be observed at the bottom left corner, and the higher temperature zone is located at the top right corner. As this figure demonstrates, the maximum temperature was +81.4 °C located on the hot spot.

![Figure 3a](image1)

![Figure 3b](image2)

![Figure 3c](image3)

![Figure 3d](image4)

**Figure 3.** Temperature distribution in case 1 (uniform heat flux of the hot spot was 1500 W cm\(^{-2}\)); a) entire cooling design, b) top surface of the chip, c) microchannels, and d) five slices of the entire model.
Figure 4 show the coolant velocity distribution in microchannels. Maximum velocity in microchannels was 3.1 m s$^{-1}$. In figure 4b, a sliced view of cooling design is shown in such a way that velocity contours of channel #10 of the first layer can be seen. This channel was immediately under the hot spot. As this figure shows, laminar boundary layer thickness increases as flow moves toward the exit. Thus, the value of maximum velocity increases accordingly to satisfy the conservation of mass at each section along the x-direction.

**FIGURE 4.** Coolant velocity distribution in case 1 (uniform heat flux of the hot spot is 1500 W cm$^{-2}$); a) microchannels, and b) a slice view of velocity contours.

In case 2, a uniform thermal load of 2000 W cm$^{-2}$ was applied on the hot spot. Figure 5a shows temperature variations on the entire cooling design. The maximum temperature in this case increased to +91.7 $^\circ$C, which was 10.3 $^\circ$C higher than in case 1. The minimum temperature on this surface was the same as the minimum temperature in case one, which was +43.2 $^\circ$C. As this figure illustrates, the effect of the second microchannel layer in this case also was not significant compared to the first layer. In this case, higher temperature gradients are observed close to the hot spot compared to case 1 (figure 5b). This demonstrates that by increasing the heat load on the hot spot, effectiveness of the microchannel cooling decreases. Figure 5c shows the temperature distribution on microchannel walls. Figure 5c shows that the maximum temperature of microchannel walls in this case increased to +82.5$^\circ$C, which was 8.1 $^\circ$C more than the case 1. From the sliced view shown in figure 5d, a larger temperature gradient can be observed under the hot spot.

The velocity distribution in microchannels for case 2 is shown in figure 6. Since the inlet velocities in both cases are the same, almost the same velocity distribution can be seen in both cases. Maximum velocity in microchannels was also 3.1 ms$^{-1}$. 
FIGURE 5. Temperature distribution in case 2 (uniform heat flux of the hot spot is 2000 W cm\(^{-2}\)); a) entire cooling design, b) top surface of the chip, c) microchannels, and d) five slices of the entire model.

FIGURE 6. Velocity distribution in case 2 (uniform heat flux of the hot spot is 2000 W cm\(^{-2}\)); a) microchannels, and b) a slice view of the microchannels.

To further study the heat removal capacity of this two-layer microchannel based system, the heat fluxes on the bottom surface are plotted in figure 7. Very similar patterns for the heat flux distributions can be seen in both cases. However, case 2 had slightly higher heat fluxes, especially at the center of the bottom surface. By comparing figure 7 with figure 2 and 4, it can be observed that the minimum heat flux magnitude on the bottom surface occurred at sides where the inlets are located. Consequently, the maximum of heat flux magnitude was on the top right of this surface where water exited from both layers of microchannels.

Figure 7. Heat flux at the bottom surface of the microchannels; a) case 1, b) case 2.
The magnitude of average heat flux on the bottom surface for case 1 was 219.62 W cm\(^{-2}\), and for case 2 was 224.83 W cm\(^{-2}\). The difference between these heat fluxes and the applied heat flux is the amount of heat flux removed by water. Table 1 shows the ratio of percentage of the heat removed by fluid (convection heat transfer) over the total heat load in both cases.

<table>
<thead>
<tr>
<th>Design</th>
<th>Applied heat load (W)</th>
<th>Removed heat by conduction (W)</th>
<th>Removed heat by convection (W)</th>
<th>Convection/heat load (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>61.275</td>
<td>13.495</td>
<td>48.780</td>
<td>77.976</td>
</tr>
<tr>
<td>Case 2</td>
<td>62.525</td>
<td>13.821</td>
<td>49.704</td>
<td>77.895</td>
</tr>
</tbody>
</table>

Table 1. Heat removed via convection and conduction.

As this table demonstrates in case 2, the ratio of convection heat transfer over heat load was 0.07% less than in case 1. The extra heat applied in case 2 due to 500 W cm\(^{-2}\) higher heat flux on the hot spot than in case 1 was 1.25 W. It should be noted that 74% of this extra heat was removed via convection heat transfer. This percentage was calculated by dividing the convection heat transfer difference between case 1 and case 2, over the extra heat on the hot spot in case 2, which was 1.25 W. The rest of this extra heat was transferred to the bottom surface via conduction heat transfer. This causes 0.08% reduction in the ratio of convection heat transfer over heat load in case 2. By using multi-objective optimization method the location and aspect ratio of microchannels can be optimized in order to enhance the convection heat transfer in this cooling system. Moreover, direction and inlet velocity of fluid flow and number of layers of microchannels can also be considered as two design variables for such a study to increase the temperature uniformity on the top surface.

4. STRESS ANALYSIS

Steady state linear stress analysis was also performed to determine the thermal stresses due to temperature variations within this cooling design. COMSOL Multiphysics 3D stress-deformation solver was linked to its conjugate heat transfer solver for these simulations. This means the temperature field obtained from conjugate heat transfer analysis was used for thermal stress calculations. Following boundary conditions were used for simulations:

1. Zero displacement (fixed) wall for the top surface,
2. Free wall for other external walls and all microchannels’ walls.

The top surface was assumed to be a fixed wall since it should be connected to the chip.

In this paper, von Mises stress was used to study stresses inside the entire cooling configuration. Figures 8a shows the von Mises stress distribution for the case 1. The maximum von Mises stress for this case was 92 MPa. Larger von Mises stresses can be seen at the edges above the outlets of the first microchannel layer due to higher temperature gradients. Figure 8b shows that the maximum von Mises stress on the top surface of the substrate was 17 MPa less than the global maximum of this stress shown in figure 8a. The distribution of von Mises stress on the channels walls is shown figure 8c where higher von Mises stresses can be observed on the top surfaces of the first microchannel layer near the outlets. This was because of larger temperature gradients between the fluid inside the channels and its upper wall near the outlets. Figure 8d illustrates 5 sliced views (along the z-direction) for the von Mises stress. It should be noticed that these slices were located between channels of the first layer at equally spaced intervals. There were significant decrements in von Mises stresses on the top wall of channels (figure 8c) and the area between channels. Maximum stress in figure 8d located at top corners close to the outlet. The middle slice (slice #3) shows higher von Mises stresses under the hot spot.
Von Mises stresses for case 2 are shown in figure 9. The maximum stress in this case was 10 MPa higher than in case 1. The reason for this increment is due to slightly higher temperature gradients in case 2 compared to case 1. Figure 9c illustrates that by increasing the hot spot heat flux to 2000 W cm$^{-2}$, the von Mises stress increases at the top walls of channels under the hot spot. Meanwhile, the distribution pattern of the von Mises stress in the rest of cooling design remained almost the same as the case 1.

Considering the very high yield strength of silicon (7 GPa, [19]), the range of von Mises stress were in a safe zone. However, the displacements caused by thermal stresses were also studied to examine the robustness of this cooling design in handling thermal deformations. Figure 10a shows the displacement distribution in entire cooling design for case 1. The maximum displacement in this case was 56.6 nm which occurred at the outlet of both microchannel layers where there are higher temperature gradients in the y-direction (figure 3a).
Figure 9. Stress distribution on case 2 (uniform heat flux of the hot spot is 2000 \( \text{W cm}^{-2} \)); a) entire cooling design, b) the top surface of the chip, c) microchannels and d) five slices of the entire model.

Figure 10b shows the deformation in five sliced views (along the x-direction) of microchannel cooling configuration for the case 1. The region above the first microchannel layer had smaller deformations. Figure 10c and 10d illustrate the displacements in case 2. The maximum deformation in case 2 is almost the same as in case 1. However, from figure 10d (slice #3), larger displacements can be observed under the hot spot.

5. CONCLUSIONS AND RECOMMENDATIONS

In this research, 3-D conjugate heat transfer and stress analyses were performed to numerically investigate effects of two-layer single phase flow microchannels for cooling electronic chips having a hot spot with up to 2000 \( \text{W cm}^{-2} \) thermal loads. The thermal load of 1000 \( \text{W cm}^{-2} \) was applied on
the rest of the top surface of the chip. Results of case 1 in which the thermal load of the hot spot was 1500 W cm$^{-2}$ showed that the maximum temperature on the top surface of the chip was +81.4 °C. Results of case 2 in which the hot spot thermal load was 2000 W cm$^{-2}$ showed maximum temperature of the hot spot was increased by 10.3 °C to +91.7 °C. This shows that the proposed two-layer microchannel configuration can handle 1000 W cm$^{-2}$ background thermal load with a moderate hot spot thermal load. Higher background thermal loads and higher hot spot thermal loads will require multi-objective constrained design optimization of topology of the cooling microchannels, different cooling fluid, introduction of a very thin layer of diamond or nanoplatelets based high thermal conductivity heat spreaders, and altogether different cooling concepts in order to keep the hot spot temperature below +85 °C. Linear stress analysis results indicate that the von Mises stresses and the deformation due to temperature gradient are within an acceptable range for both cases analysed here.

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