# Abas Abdoli

MAIDROC Laboratory, Department of Mechanical and Materials Engineering, Florida International University, Miami, FL 33174 e-mail: aabdo004@fiu.edu

# George S. Dulikravich

MAIDROC Laboratory, Department of Mechanical and Materials Engineering, Florida International University, Miami, FL 33174 e-mail: dulikrav@fiu.edu

# **Genesis Vasquez**

MAIDROC Laboratory, Department of Mechanical and Materials Engineering, Florida International University, Miami, FL 33174 e-mail: gvasq007@fiu.edu

# Siavash Rastkar

MAIDROC Laboratory, Department of Mechanical and Materials Engineering, Florida International University, Miami, FL 33174 e-mail: srast002@fiu.edu

# Thermo-Fluid-StressDeformation Analysis of Two-Layer Microchannels for Cooling Chips With Hot Spots

Two-layer single phase flow microchannels were studied for cooling of electronic chips with a hot spot. A chip with  $2.45 \times 2.45$  mm footprint and a hot spot of  $0.5 \times 0.5$  mm in its center was studied in this research. Two different cases were simulated in which heat fluxes of  $1500 \text{ W cm}^{-2}$  and  $2000 \text{ W cm}^{-2}$  were applied at the hot spot. Heat flux of  $1000 \text{ W cm}^{-2}$  was applied on the rest of the chip. Each microchannel layer had 20 channels with an aspect ratio of 4:1. Direction of the second microchannel layer was rotated 90 deg with respect to the first layer. Fully three-dimensional (3D) conjugate heat transfer analysis was performed to study the heat removal capacity of the proposed two-layer microchannel cooling design for high heat flux chips. In the next step, a linear stress analysis was performed to investigate the effects of thermal stresses applied to the microchannel cooling design due to variations of temperature field. Results showed that two-layer microchannel configuration was capable of removing heat from high heat flux chips with a hot spot. [DOI: 10.1115/1.4030005]

Keywords: electronics cooling, single phase flow microchannel, hot spot

### 1 Introduction

Thermal management challenges facing electronic cooling developers [1,2] are currently at the confluence of chip power dissipation well above 100 W cm<sup>-2</sup> as background heat flux and localized hot spots with more than 1000 W cm<sup>-2</sup> fluxes. Sahu et al. [3] applied a hybrid cooling scheme which combines microfluidic and solid-state cooling techniques in cooling hot spots with heat flux close to 250 W cm<sup>-2</sup>. In another research, Sahu et al. [4] studied a liquid-thermoelectric hybrid cooling method for hot spots with heat fluxes more than 600 W cm<sup>-2</sup>. They reported that liquid-thermoelectric hybrid cooling showed better results for higher heat fluxes at hot spots. Alfieri et al. [5,6] numerically investigated hot spot cooling in 3D stacked chips with integrated cooling. They studied the influence and implications of the integrated water-cooling, through-silicon-via (TSV) distribution, and size on the control of inhomogeneous hot spots. Zhang et al. [7,8] experimentally investigated effects of silicon micro pin-fin heat sink with integrated TSVs in cooling high power chips. Sullivan et al. [9] proposed the use of an array of thermoelectric coolers for thermal management of chips with hotspot heat flux of 1000 and background heat flux of 43 W cm<sup>-2</sup>. Redmond and Kumar [10] optimized the thermoelectric material thickness for the hot spot and background heat fluxes of 1000 W cm<sup>-2</sup> and 14.5 W cm<sup>-2</sup>, respectively.

Abdoli and Dulikravich [11] performed multi-objective optimization for four-layer branching microchannel configurations

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received June 20, 2014; final manuscript received March 2, 2015; published online April 16, 2015. Assoc. Editor: Mehmet Arik.

with 67 design variables to improve heat removal and decrease temperature nonuniformity and coolant pumping pressure drop. They also numerically optimized the multilayer through-flow microchannels for heat fluxes up to 800 W cm<sup>-2</sup> [12]. Genetic algorithms have been used by Wei and Joshi [13] to perform single objective optimization in order to minimize overall thermal resistance. Li and Peterson [14] applied full 3D numerical simulations to find the optimal geometric conditions in parallel microchannels with heat fluxes of 100 W cm<sup>-2</sup>. In a recent research, Abdoli et al. [15] performed fully 3D conjugate hydrothermal analysis of arrays of micro pin-fin shapes (cylindrical, hydrofoil, modified hydrofoil, and convex lens) with different sizes in cooling of chips with hot spot heat flux of 2000 W cm<sup>-2</sup> and background heat flux of 1000 W cm<sup>-2</sup>.

The main advantages of using straight through-flow cooling channels rather than branching cooling channels are: (a) lower pumping power requirements, (b) lower manufacturing cost, (c) better uniformity of hot surface temperature, and (d) higher reliability in case of blockage in any of the microchannels. In the present paper, a cooling configuration with two-layers of straight microchannels was investigated numerically. The chip included a hot spot with heat flux of 2000 W cm<sup>-2</sup> at its center. Stress analysis was also performed to study thermal stresses due to temperature variations.

# 2 Two-Layer Microchannel Cooling Design Including a Hot Spot

A two-layer microchannel configuration was designed for a chip with  $2.45 \times 2.45$  mm footprint, shown in Fig. 1. Each channel had the cross section dimensions of  $240 \times 60$   $\mu$ m (height and

Journal of Electronic Packaging

Copyright © 2015 by ASME

SEPTEMBER 2015, Vol. 137 / 031003-1

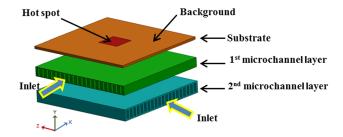


Fig. 1 Expanded view of two-layer microchannel cooling design

width). This allowed more microchannels to be located in each layer. Each microchannel layer consisted of 20 channels. As this figure shows, direction of the second layer was rotated 90 deg with respect to the first layer. The reason was to enhance the heat transfer from the chip. Substrate, first and second layers of microchannels were all assumed to be made from silicon. A hot spot with size of  $500 \times 500~\mu m$  was located at the center of the substrate top surface. Considering the size of chip, this hot spot is considered to be large which will be challenging for the cooling system. The chip size was constrained by limitations in computational resources for simulating such configurations.

comsol multiphysics software was used for meshing the configuration. This cooling design configuration consists of 40 fluid domains and one solid domain. A fine 3D hybrid computational grid was used for finite element simulations. Each of the 40 microchannels was discretized with 20,000 3D grid cells, and the rest of the cooling design was discretized with 600,000 3D grid cells. Grid independency analysis was performed by using a finer mesh with larger number of computational cells for each domain. The total number of grid cells for each channel was increased from 20,000 to 25,000 and for the rest of the design from 600,000 to 700,000. Variations of thermofluid results between both cases were less than 1.3%.

Figure 2 illustrates the hybrid grid in the entire solution domains. The enlarged view demonstrates the concentration of grid cells near edges. In this study, considering the applied Reynolds number (<290), flow pattern inside microchannels was assumed to be laminar [16,17]. Therefore, not having a very fine mesh adjacent to the internal walls was acceptable since the flow was not turbulent.

### 3 Conjugate Heat Transfer Analysis

Multidomain steady-state conjugate heat transfer analysis was performed to study the temperature distribution using a two-layer microchannel configuration. In this study, water was used as the cooling liquid. Hydraulic diameter (characteristic length) of microchannel was calculated as the square root of cross section area [16], 120  $\mu$ m. The Knudsen number for a fluid is defined based on the lattice spacing,  $\delta$  [18,19]

$$Kn = \frac{\delta}{L} \tag{1}$$

where L is the characteristic microchannel dimension (hydraulic diameter). The value of  $\delta$  for water is 0.3 nm. Janson et al. [20] and Gad-el-Hak [21] reported that for Knudsen numbers greater than  $10^{-3}$ , the equilibrium assumption is not valid. Gad-el-Hak [21] suggested applying modified slip boundary conditions in continuum models for Knudsen numbers between  $10^{-1}$  and  $10^{-3}$ . For fluid flows with Knudsen numbers in this range or above, the continuum assumption and classical fluid theory are no longer applicable [20,21]. The calculated Knudsen number for microchannels in this paper was  $2.5 \times 10^{-6}$ , which was below  $10^{-3}$ . Thus, classical Navier–Stokes equations were used. The following are Navier–Stokes equations for steady state, incompressible flow:

$$\nabla \cdot \mathbf{V} = 0 \tag{2}$$

$$\rho(\mathbf{V} \cdot \nabla)\mathbf{V} = \nabla \cdot \left[ -p\mathbf{I} + \mu \Big( \nabla \mathbf{V} + (\nabla \mathbf{V})^{\mathrm{T}} \Big) \right] + \mathbf{F}$$
 (3)

The conservation of energy for incompressible flow (with viscous dissipation neglected) has the form

$$\rho C_{p}(\mathbf{V} \cdot \nabla)T = (\mathbf{V} \cdot \nabla)p + \nabla \cdot (k\nabla T) + \rho \dot{q} \tag{4}$$

For the solid domain, the velocity will be explicitly enforced as equal to zero. Forty 3D fluid domains and one solid domain were coupled and simulated using COMSOL multiphysics conjugated heat transfer finite element solver. This model was validated versus experimental data by different researchers [22,23].

Inlet averaged velocity was assumed to be 2 m s<sup>-1</sup>. Therefore, the inlet Reynolds number was 287.4. The water inlet temperature was set to 26.8 °C, which is close to the room temperature. The outlet static pressure was specified as 110 kPa which is near to the atmospheric pressure. Two different cases were simulated. In case 1, a uniform thermal load of 1500 W cm<sup>-2</sup> was applied at the hot spot. In case 2, a uniform heat flux of 2000 W cm<sup>-2</sup> was applied to the hot spot. Thermal boundary conditions were:

- (1) constant bottom surface temperature:  $26.8\,^{\circ}\text{C}$
- (2) constant background heat flux (excluding hot spot):  $1000~{\rm W~cm}^{-2}$
- (3) constant heat flux on hot spot, case 1: 1500 W cm $^{-2}$  and case 2: 2000 W cm $^{-2}$
- (4) adiabatic surface for all sidewalls

It was assumed that the bottom surface temperature can be maintained near the room temperature  $(26.8\,^{\circ}\text{C})$  via external cooling. Also, it was assumed that heat transfer from sidewalls was negligible (adiabatic surfaces). This way, all heat should be removed by the cooling liquid via convection or via conduction from the bottom surface. Figure 3(a) illustrates the calculated temperature distribution inside the substrate and coolant for case 1. The water flow direction in the first layer was in the *x*-direction.

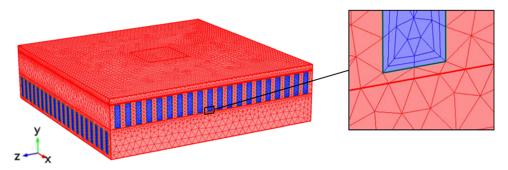


Fig. 2 Hybrid computational grid with an enlarged view

031003-2 / Vol. 137, SEPTEMBER 2015

Transactions of the ASME

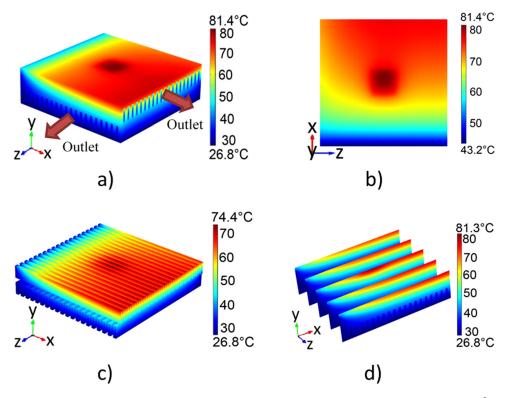


Fig. 3 Temperature distribution in case 1 (uniform heat flux of the hot spot was 1500 W cm $^{-2}$ ): (a) entire cooling design, (b) top surface of the chip, (c) microchannels, and (d) five slices of the entire model

In the second layer, due to a 90 deg rotation with respect to the first layer, water was pumped in the direction of z-axis. As Figure 3(a) illustrates, temperature variations in the second microchannel layer were not significant. In other words, this layer did not play a noticeable role in this cooling system. As water moves toward the outlets, its temperature increases.

Figure 3(b) shows variations of temperature on the top surface of silicon substrate. Due to the 90 deg shift in the flow directions, a lower temperature zone can be observed at the bottom left corner, and the higher temperature zone is located at the top right corner. As this figure demonstrates, the maximum temperature was  $81.4\,^{\circ}\text{C}$  located on the hot spot. Figure 3(c) shows the temperature distributions on microchannels. It can be observed that top surfaces of channels under the hot spot had higher temperatures compared to other channels. To better illustrate the temperature variations of this cooling design in the z-direction, five sliced views in this direction are shown in Fig. 3(d). It can be seen that the third slice which was located under the hot spot had higher temperatures and higher temperature gradients, especially near the top surface.

Figure 4 shows the coolant velocity distribution in microchannels. Maximum velocity in microchannels was  $3.1 \text{ m s}^{-1}$ . In Fig. 4(b), a sliced view of cooling design is shown in such a way that velocity contours of channel number ten of the first layer can be seen. This channel was immediately under the hot spot. As this figure shows, laminar boundary layer thickness increases as flow moves toward the exit. Thus, the value of maximum velocity increases accordingly to satisfy the conservation of mass at each section along the *x*-direction.

In case 2, a uniform thermal load of 2000 W cm<sup>-2</sup> was applied on the hot spot. Figure 5(a) shows temperature variations on the entire cooling design. The maximum temperature in this case increased to 91.7 °C, which was 10.3 °C higher than in case 1. The minimum temperature on this surface was the same as the minimum temperature in case one, which was 43.2 °C. As this figure illustrates, the effect of the second microchannel layer in this case also was not significant compared to the first layer. In this case, higher temperature gradients are observed close to the hot spot compared to case 1 (Fig. 5(b)). This demonstrates that by increasing the heat load on the hot spot, effectiveness of the

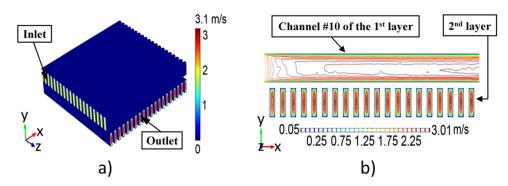


Fig. 4 Coolant velocity distribution in case 1 (uniform heat flux of the hot spot is 1500 W  $cm^{-2}$ ): (a) microchannels and (b) a slice view of velocity contours

Journal of Electronic Packaging

SEPTEMBER 2015, Vol. 137 / 031003-3

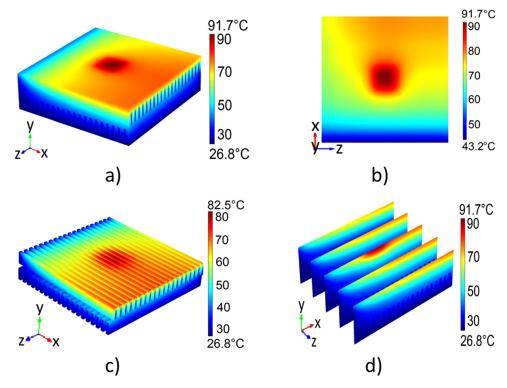


Fig. 5 Temperature distribution in case 2 (uniform heat flux of the hot spot is 2000 W cm $^{-2}$ ): (a) entire cooling design, (b) top surface of the chip, (c) microchannels, and (d) five slices of the entire model

microchannel cooling decreases. Figure 5(c) shows the temperature distribution on microchannel walls. Figure 5(c) shows that the maximum temperature of microchannel walls in this case increased to  $82.5\,^{\circ}\mathrm{C}$ , which was  $8.1\,^{\circ}\mathrm{C}$  more than the case 1. From the sliced view shown in Fig. 5(d), a larger temperature gradient can be observed under the hot spot.

The velocity distribution in microchannels for case 2 is shown in Fig. 6. Since the inlet velocities in both cases are the same, almost the same velocity distribution can be seen in both cases. Maximum velocity in microchannels was also 3.1 m s<sup>-1</sup>. The maximum temperature can be decreased by increasing the inlet velocity. However, convection heat transfer alone will not be capable of removing the applied heat at the hot spot and keeping the maximum temperature below 80 °C. The main reason is coolant boundary layers close to the walls which decrease the convection heat transfer effect. One solution to decrease the maximum temperature is to increase the thickness of the channel's walls in this region to enhance conduction heat transfer. This way more heat will be transferred to the second layer and the second layer will be more efficient.

To further study the heat removal capacity of the two-layer microchannel based cooling system; the heat fluxes on the bottom surface are plotted in Fig. 7. Very similar patterns for the heat flux distributions can be seen in both cases. However, case 2 had slightly higher heat fluxes, especially at the center of the bottom surface. By comparing Fig. 7 with Figs. 2 and 4, it can be observed that the minimum heat flux magnitude on the bottom surface occurred at the sides where the inlets are located. Consequently, the maximum heat flux magnitude was on the top right of this surface where water exited from both layers of microchannels.

The magnitude of average heat flux on the bottom surface for case 1 was 219.62 W cm<sup>-2</sup> and for case 2 was 224.83 W cm<sup>-2</sup>. The difference between these heat fluxes and the applied heat flux is the amount of heat flux removed by water. Table 1 shows the ratio of percentage of the heat removed by fluid (convection heat transfer) over the total heat load in both cases which are indications of their thermal efficiencies.

As this table demonstrates in case 2, the ratio of convection heat transfer over heat load was 0.07% less than in case 1. The external heat applied in case 2 due to 500 W cm<sup>-2</sup> higher heat

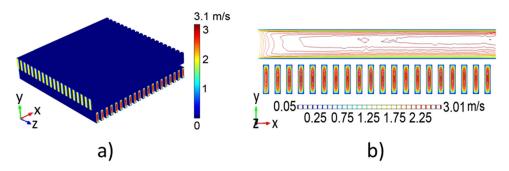


Fig. 6 Velocity distribution in case 2 (uniform heat flux of the hot spot is 2000 W cm<sup>-2</sup>): (a) microchannels and (b) a slice view of the microchannels

031003-4 / Vol. 137, SEPTEMBER 2015

**Transactions of the ASME** 

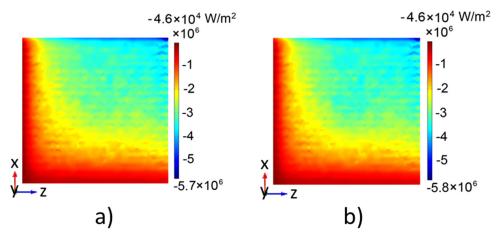


Fig. 7 Heat flux at the bottom surface of the microchannels: (a) case 1 and (b) case 2

Table 1 Heat removed via convection and conduction

Design	Applied heat load (W)	Removed heat by conduction (W)	Removed heat by convection (W)	Convection/heat load (%)	Pumping power (W)
Case 1	61.275	13.495	48.780	77.976	0.018
Case 2	62.525	13.821	49.704	77.895	0.018

flux on the hot spot compared to case 1 was 1.25 W. Seventy-four percent of this external heat was removed via convection heat transfer. This percentage was calculated by dividing the convection heat transfer difference between case 1 and case 2, over the external heat on the hot spot in case 2, which was 1.25 W. The rest of this external heat was transferred to the bottom surface via conduction heat transfer. This causes a slight reduction of 0.08% in the ratio of convection heat transfer over heat load in case 2.

The required pumping powers were also calculated and presented in Table 1. The average inlet pressure was used in pumping power calculation. Pumping power in both cases was the same and equals to 0.018 W. The average Nusselt number,  $\overline{\text{Nu}}_{\sqrt{A}}$ , was calculated based on the total heat removed by fluid in each microchannel, average temperature of water, and average temperature of channel walls. Square root of the cross-sectional area of microchannel was used as the characteristic length in Nusselt number calculation [16]. Nusselt number for all channels in case 1 was approximately 7.62, which was very close to the one in case 2, 7.63. This was due to the same Reynolds number, dimensions, and type of coolant in both cases. Friction factor of the channels in the first layer was 0.28 and for the channels in the second layer was 0.33. The reason for the difference between the friction factors of the first and second layers was the temperature dependence of water thermal properties. The same results were obtained for case 2. By using multi-objective optimization method, the location and aspect ratio of microchannels can be optimized in order to enhance the convection heat transfer in this cooling system. Moreover, direction and inlet velocity of fluid flow and number of layers of microchannels can also be considered as two design variables for such a study to increase the temperature uniformity on the top surface. Thickness of microchannel's walls can also be the additional design variable.

### 4 Stress and Deformation Analysis

Steady-state linear stress analysis was also performed to determine the thermal stresses due to temperature variations within this cooling design. This means that the temperature field obtained from conjugate heat transfer analysis was used for thermal stress calculations. The conservation of momentum for a homogeneous solid body element [24] can be written as

$$\rho \frac{\partial^2 \mathbf{u}}{\partial t^2} - \nabla \cdot \Sigma - \mathbf{F} = 0 \tag{5}$$

For a linear elastic solid, stress tensor,  $\Sigma$ , can be written as

$$\Sigma = 2GE + \lambda tr(E)I \tag{6}$$

where  $\lambda$  and G can be determined by using

$$\lambda = \frac{Ev}{(1+v)(1-2v)}$$
 and  $G = \frac{E}{2(1+v)}$  (7)

The combined strain tensor,  $\varepsilon$ , is defined as

$$E = \frac{1}{2} [\nabla \mathbf{u} + (\nabla \mathbf{u})^{T}] + \alpha_{v} (\Delta T) \mathbf{I} \text{ where } \Delta T = T - T_{0}$$
 (8)

Here, superscript T denotes the transpose. Combining Eqs. (5), (6), and (8), the governing equation for an isotropic, homogenous, solid body with no motion and no external body forces, becomes

$$\nabla \cdot \left[ G \left( \nabla \mathbf{u} + (\nabla \mathbf{u})^{\mathsf{T}} + 2\alpha_{\mathsf{v}}(\Delta \mathsf{T})\mathbf{I} \right) + \lambda \operatorname{tr}(\nabla \mathbf{u} + \alpha_{\mathsf{v}}(\Delta \mathsf{T})\mathbf{I}) \right] = 0$$
(9)

COMSOL multiphysics 3D stress-deformation solver was linked to its conjugate heat transfer solver for these simulations. Following boundary conditions were used for simulations:

- (1) zero displacement (fixed) wall for the top surface
- (2) free wall for other external walls and all microchannels' walls

The top surface was assumed to be a fixed wall since it should be connected to the chip.

In this paper, von Mises stress was used to study stresses inside the entire cooling configuration.

Figure 8(a) shows the von Mises stress distribution for case 1. The maximum von Mises stress for this case was 92 MPa. Larger von Mises stresses can be seen at the edges above the outlets of

SEPTEMBER 2015, Vol. 137 / 031003-5

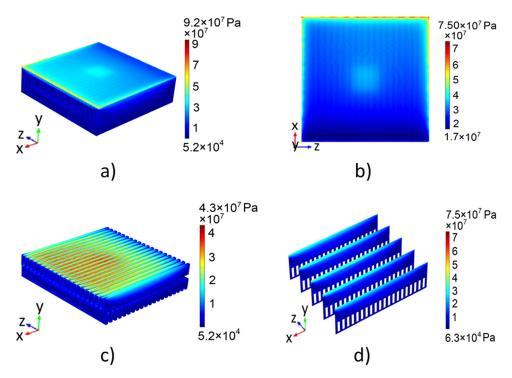


Fig. 8 Stress distribution for case 1 (uniform heat flux of the hot spot is 1500 W cm $^{-2}$ ): (a) entire cooling design, (b) top surface of the chip, (c) microchannels, and (d) five slices of the entire model

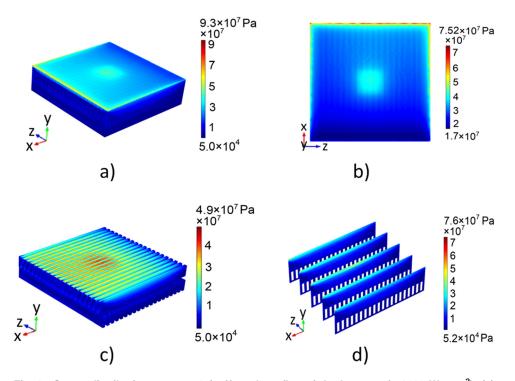


Fig. 9 Stress distribution on case 2 (uniform heat flux of the hot spot is 2000 W cm $^{-2}$ ): (a) entire cooling design, (b) the top surface of the chip, (c) microchannels, and (d) five slices of the entire model

the first microchannel layer due to higher temperature gradients. Figure 8(b) shows that the maximum von Mises stress on the top surface of the substrate was 17 MPa less than the global maximum of this stress shown in Fig. 8(a). The distribution of von Mises stress on the channel's walls is shown in Fig. 8(c), where higher von Mises stresses can be observed on the top surfaces of the first

microchannel layer near the outlets. This was because of larger temperature gradients between the fluid inside the channels and its upper wall near the outlets. Figure 8(d) illustrates five sliced views (along the z-direction) for the von Mises stress. It should be noticed that these slices were located between channels of the first layer at equally spaced intervals. There were significant

031003-6 / Vol. 137, SEPTEMBER 2015

Transactions of the ASME

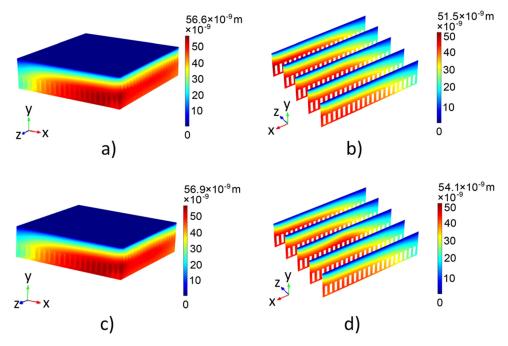


Fig. 10 Displacement distribution: (a) entire cooling design in case 1, (b) five sliced views in case 1, (c) entire cooling design in case 2, and (d) five sliced views in case 2

decrements in von Mises stresses on the top wall of channels (Fig. 8(c)) and the area between channels. Maximum stress in Fig. 8(d) is located at top corners toward the first layer's outlet. The middle slice (slice #3) shows higher von Mises stresses under the hot spot.

Von Mises stresses for case 2 are shown in Fig. 9. The maximum stress in this case was 10 MPa higher than in case 1. The reason for this increment is due to slightly higher temperature gradients in case 2 compared to case 1. Figure 9(c) illustrates that by increasing the hot spot heat flux to 2000 W cm<sup>-2</sup>, the von Mises stress increases at the top walls of channels under the hot spot. Meanwhile, the distribution pattern of the von Mises stress in the rest of the cooling design remained almost the same as case 1.

Considering the very high yield strength of silicon (7 GPa, [25]), the range of von Mises stress was in a safe zone. However, the displacements caused by thermal stresses were also studied to examine the robustness of this cooling design in handling thermal deformations. Figure 10(a) shows the displacement distribution in the entire cooling design for case 1. The maximum displacement in this case was 56.6 nm which occurred at the outlet of both microchannel layers where there are higher temperature gradients in the y-direction (Fig. 3(a)).

Figure 10(b) shows the deformation in five sliced views (along the *x*-direction) of microchannel cooling configuration for case 1. The region above the first microchannel layer had smaller deformations. Figures 10(c) and 10(d) illustrate the displacements in case 2. The maximum deformation in case 2 is almost the same as in case 1. However, from Fig. 10(d) (slice #3), larger displacements can be observed under the hot spot.

# 5 Conclusions and Recommendations

In this research, 3D conjugate heat transfer and stress analyses were performed to numerically investigate effects of two-layer single phase flow microchannels for cooling electronic chips having a hot spot with up to 2000 W cm $^{-2}$  thermal loads. The thermal load of 1000 W cm $^{-2}$  was applied on the rest of the top surface of the chip. Results of case 1 in which the thermal load of the hot spot was 1500 W cm $^{-2}$  showed that the maximum temperature on the top surface of the chip was  $81.4\,^{\circ}\text{C}$ . Results of case 2 in which

the hot spot thermal load was 2000 W cm<sup>-2</sup> showed that maximum temperature of the hot spot was 10.3 °C higher than in case 1. This shows that the proposed two-layer microchannel configuration can handle 1000 W cm<sup>-2</sup> background thermal load with a moderate hot spot thermal load. Higher thermal loads will require multi-objective constrained design optimization of topology of the cooling microchannels, different cooling fluid, introduction of a very thin layer of diamond or nanoplatelets-based high thermal conductivity heat spreaders, and altogether new cooling concepts in order to keep the hot spot temperature below 85 °C. Linear stress analysis results indicated that the von Mises stresses due to temperature gradients were an order of magnitude smaller than the yield strength of silicon. The maximum deformation was approximately 50 nm.

## Acknowledgment

Authors are grateful for partial financial support of this research provided by the DARPA via GaTech in the framework of ICE-Cool project under supervision of Dr. Avram Bar-Cohen. The lead author would like to acknowledge the financial support of a Florida International University Dissertation Year Fellowship. The authors also gratefully acknowledge the FIU Instructional and Research Computing Center for providing HPC resources to perform calculations for this project.

### Nomenclature

 $C_p$  = specific heat per unit mass at constant pressure

 $\vec{E} = \hat{Y}$ oung's modulus of elasticity

F =body force vector per unit volume

G = Lamé's second coefficient

I = identity matrix

k =thermal conductivity

L = characteristic length

p = pressure

q = heat source per unit mass

T = absolute temperature

 $T_0$  = reference absolute temperature

 $\mathbf{u} = \text{solid displacement vector}$ 

 $V = velocity\ vector$ 

Journal of Electronic Packaging SEPTEMBER 2015, Vol. 137 / 031003-7

# **Greek Symbols**

- $\alpha_{\rm v} =$  thermal diffusivity
- $\delta$  = lattice spacing
- E = strain tensor
- $\lambda = \text{Lamé's first parameter}$
- $\mu = dynamic viscosity$
- v = Poisson's ratio
- $\rho = \text{density}$
- $\Sigma$  = stress tensor

### References

- [1] Bar-Cohen, A., 2013, "Gen-3 Thermal Management Technology: Role of Microchannels and Nanostructures in an Embedded Cooling Paradigm," ASME J. Nanotechnol. Eng. Med., 4(2), p. 020907.
- [2] Sahu, V., Joshi, Y., and Fedorov, A., 2009, "Hybrid Solid State/Fluidic Cooling for
- Hot Spot Removal," Nanoscale Microscale Thermophys. Eng., 13(3), pp. 135–150.
  [3] Sahu, V., Joshi, Y. K., and Fedorov, A. G., 2010, "Experimental Investigation of Hotspot Removal Using Superlattice Cooler," 12th IEEE Intersociety Conference Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Las Vegas, NV, June 2-5.
- [4] Sahu, V., Fedorov, A. G., Joshi, Y., Yazawa, K., Ziabari, A., and Shakouri, A., 2012, "Energy Efficient Liquid-Thermoelectric Hybrid Cooling for Hot-Spot Removal," 28th Annual IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), San Jose, CA, Mar. 18-22, pp. 130-134.
- [5] Alfieri, F., Tiwari, M. K., Zinovik, I., Poulikakos, D., Brunschwiler, T., and Michel, B., 2010, "3D Integrated Water Cooling of a Composite Multilayer Stack of Chips," ASME J. Heat Transfer, 132(12), p. 121402.
- [6] Alfieri, F., Gianini, S., Tiwari, M. K., Brunschwiler, T., Michel, B., and Poulikakos, D., 2014, "Computational Modeling of Hot-Spot Identification and Control in 3-D Stacked Chips With Integrated Cooling," Numer. Heat Transfer, Part A, 65(3), pp. 201–215.
- [7] Zhang, Y., Dembla, A., and Bakir, M. S., 2013, "Silicon Micropin-Fin Heat Sink With Integrated TSVs for 3-D ICs: Tradeoff Analysis and Experimental Testing," IEEE Trans. Compon., Packag., Manuf. Technol., 3(11), pp. 1842-1850.
- Zhang, Y., Zheng, L., and Bakir, M. S., 2013, "3-D Stacked Tier-Specific Microfluidic Cooling for Heterogeneous 3-D ICs," IEEE Trans. Compon., Packag., Manuf. Technol., 3(11), pp. 1811–1819.
- [9] Sullivan, O., Gupta, M. P., Mukhopadhyay, S., and Kumar, S., 2012, "Array of Thermoelectric Coolers for On-Chip Thermal Management," ASME J. Electron. Packag., 134(2), p. 021005.

- [10] Redmond, M., and Kumar, S., 2014, "Optimization of Thermoelectric Coolers for Hotspot Cooling in Three-Dimensional Stacked Chips," ASME J. Electron. Packag., 137(1), p. 011006.
- [11] Abdoli, A., and Dulikravich, G. S., 2014, "Multi-Objective Design Optimization of Branching, Multifloor, Counterflow Microheat Exchangers," ASME J. Heat Transfer, 136(10), p. 101801.
- [12] Abdoli, A., and Dulikravich, G. S., 2014, "Optimized Multi-Floor Throughflow Micro Heat Exchangers," Int. J. Therm. Sci., 78, pp. 111–123.

  [13] Wei, X., and Joshi, Y., 2002, "Optimization Study of Stacked Micro-Channel
- Heat Sinks for Micro-Electronic Cooling," Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM, 2002), San Diego, CA, June 1, pp. 441–448. [14] Li, J., and Peterson, G. P., 2007, "3-Dimensional Numerical Optimization of
- Silicon-Based High Performance Parallel Microchannel Heat Sink With Liquid Flow," Int. J. Heat Mass Transfer, **50**(15–16), pp. 2895–2904.
- [15] Abdoli, A., Jimenez, G., and Dulikravich, G. S., 2015, "Thermo-Fluid Analysis of Micro Pin-Fin Array Cooling Configurations for High Heat Fluxes With a Hot Spot," Int. J. Therm. Sci., 90, pp. 290-297.
- [16] Muzychka, Y. S., Duan, Z. P., and Yovanovich, M. M., 2011, "Fluid Friction and Heat Transfer in Microchannels," Microfluidics and Nanofluidics Handbook: Chemistry, Physics, and Life Science Principles, CRC Press, Boca Raton,
- [17] Saha, A. A., and Mitra, S. K., 2012, "Pressure-Driven Flow in Microchannels," Microfluidics and Nanofluidics Handbook: Chemistry, Physics, and Life Science Principles, CRC Press, Boca Raton, pp. 139-154.
- [18] Probstein, R. F., 1994, Physicochemical Hydrodynamics: An Introduction, 2nd ed., Wiley, New York.
- [19] Sharp, K. V., Adrian, R. J., Santiago, J. G., and Molho, J. I., 2005, "Liquid Flow in Microchannels," *The MEMS Handbook*, 2nd ed., Vol. 1, M. Gadel-Hak, ed., CRC Press, Boca Raton, Chap. 10.
- [20] Janson, S. W., Helvajian, H., and Breuer, K., 1999, "MEMS, Microengineering and Aerospace Systems," AIAA Paper No. 99-3802
- [21] Gad-el-Hak, M., 1999, "The Fluid Mechanics of Microdevices: The Freeman Scholar Lecture," ASME J. Fluids Eng. 121(1), pp. 5-33.
- [22] Almaneea, A., Summers, J., Thompson, H., and Kapur, N., 2013, "Optimal Heat Sink Fin and Cold Lid Heights for Liquid Immersed Servers," COMSOL Conference, Rotterdam, The Netherlands, Oct. 23-25, pp. 1-16.
- [23] Kumar, V., Jonnalagadda, D., Subbiah, J., and Thippareddi, H., 2007, "Conjugate Heat Transfer Analysis of an Egg," COMSOL Conference, Boston, MA, Oct. 4-6, pp. 1-6.
- [24] Hetnarski, R. B., and Eslami, M. R., 2009, Thermal Stresses-Advanced Theory and Applications, Springer, The Netherlands.
- [25] Petersen, K. E., 1982, "Silicon as a Mechanical Material," Proc. IEEE, 70(5), pp. 420-457.